III. REMARKS

1. Claims 1-12 remain in the application. Claims 1-12 have been amended.

The amendments to the claims are not limiting, are not made for reasons related to patentability, and do not raise issues of estoppel.

2. A replacement sheet for Figure 1 is included with this response.

3. Claims 2, 3-9, 11, and 12 have been amended to overcome the informalities rejections.

4. Claims 1, 2, 10, and 12 have been amended to overcome the 35 USC 112, second paragraph rejection.

5. Claim 12 has been amended to recite statutory subject matter under 35 USC 101.

6. Applicants respectfully submit that claims 1, 2, and 10 are not anticipated by Momtaz et al. (US 7,263,151, "Momtaz") under 35 USC 102(e).

Momtaz fails to disclose or suggest a bit error test unit adapted to receive the sampled comparator output signal and to determine therefrom an indication of a bit error in a sequence of the sampled comparator output signal by comparing the sampled comparator output signal against an expected comparator output signal representing the comparator output signal without error, as essentially recited by claims 1 and 10.

The present claims are directed to an integrated circuit with a bit error test capability. As usually understood in the art, a bit error ratio is defined as the number of erroneous bits received divided by the total number of bits transmitted (see for example, http://en.wikipedia.org/wiki/Bit_error_rate).

The present claims describe a bit error test unit that determines an indication of a bit error in a sequence of a sampled comparator output signal by comparing the sampled comparator output signal against an expected comparator output signal representing the comparator output signal without error.

Momtaz, on the other hand, verifies whether a recovered clock fits to the data from which it was recovered. Momtaz extracts a clock from incoming data and compares a phase of the clock with that of a delayed form of the incoming data. Momtaz further adjusts the delay of

the incoming data to minimize capacitive loading. There is no disclosure in Momtaz related to comparing a sampled comparator output signal against a signal representing the comparator output signal without error.

At least for these reasons, Applicants submit that Momtaz fails to anticipate independent claims 1 and 10 and dependent claims 2-9, 11, and 12.

For all of the foregoing reasons, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record, and are in proper form for allowance. Accordingly, favorable reconsideration and allowance is respectfully requested. Should any unresolved issues remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

The Commissioner is hereby authorized to charge payment for any fees associated with this communication or credit any over payment to Deposit Account No. 50-1078.

Respectfully submitted,

Joseph V. Gamberdell, Jr.
Reg. No. 44,695

19 Feb 2008
Date

Perman & Green, LLP
425 Post Road
Fairfield, CT 06824
(203) 259-1800
Customer No.: 2512

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being transmitted electronically, on the date indicated below, addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: 19 Feb. 2008 Signature:

Meg L. Hoffmans
Person Making Deposit